**PXL-Digital**

Professional Bachelor Electronics-ICT

**Mezzanine connector study of the ZUBoard 1CG**

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1. Inhoudsopgave

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1. Introductie

This application note delves into the characteristics of the mezzanine connector as well as its application within FPGA’s.

The utilized mezzanine connector is the Samtec QTE-020-01-F - D -A, incorporated into a SYZYGY template board. This expansion board is intended to enhance and extend the capabilities of the carrier board by leveraging its supported interfaces, facilitated through the versatile connectivity provided by the mezzanine connector.

# Connector capabilities and specifications

The ZUBOARD is equipped with three mezzanine connectors, comprising of two transceiver TXR-2 variety and one connector of the standard type.

The connectors provided with the board lack support for smart VIO functionality. The voltage needs to be managed manually.

The significant differences between the 2 types are:

* TXR-2 has more additional single-ended signals
* TXR-2 has 4 transceiver pairs and reference clock for high-performance I/O, this feature is missing on the default connector.

The connector facilitates high-speed data transfer and communication between the main board and expansion modules, offering versatility through support for a combination of analog and digital I/O interfaces for peripherals.

Key features include:

* Data Throughput: Supports high-speed single-ended and differential signaling up to 25 Gbps
* Latency: By eliminating protocol overhead, the connector ensures deterministic data delivery, minimizing latency in communication.
* Design Simplicity: Expertise in specific protocol standards such as PCI, PCI Express®, or Serial RapidIO is not a prerequisite, simplifying the design process.
* System Overhead: Simplification of the system design results in reduced power consumption, lower IP core costs, decreased engineering time, and overall material cost savings.

Moreover, the connector's versatility is highlighted by its support for various peripherals, including:

* High speed data acquisition (ADC)
* High speed DAC
* Image capture
* Software-defined radio
* Video input and output
* Multi-channel I/O
* Digital communications

This broad range of capabilities enables the exploration of diverse applications, from high-bitrate data exchanges to multimedia integration and the integration of custom expansion modules connected to specific project requirements.

# QSPI vs. connectors interface, speed comparison

Given the challenge of comparing protocols serving distinct purposes or comparing a protocol to a port, the focus will be on a comparison within serial communication protocols.

The protocols serving this purpose are:

* RS232 / RS485
* CAN
* LIN
* SPI
* I2C
* USB
* PCI Express
* Ethernet

The following Protocols with low baud rates have been excluded from the comparison:

* RS232 / RS485
* CAN
* LIN
* I2C

Quad Serial Peripheral Interface (QSPI) is a serial communication interface that uses 4 data lines namely, I0, I1, I2 and I3. QSPI is typically used in applications such as ADC converters etc. QSPI can reach throughput rates up to 40Mbit/s to a max of 100Mbit/s varying on the type.

The mezzanine connector in the standard variant can reach up to 500 MHz/pin making it compatible with protocols such as PCI Express 4.0 which can have speeds up to 16Gbit/s, usb20Gbps which as the name suggests can have speeds up to 20 Gbit/s and ethernet with speeds up to 25 Gbit/s.

Due to the resulting high bandwidths with certain interfaces, it is safe to confirm that the mezzanine connector can achieve faster communication than the one provided with QSPI.

However, the communication protocols that attain higher bandwidths are often more complex to work with. In certain scenarios they may lack the versatility to address specific serial communication challenges, making QSPI a reliable choice for tackling certain issues.

# 4 Use of the pMCU on the expansion shield

This chapter will cover the need for a peripheral MCU in the expansion board, as well as some of the characteristics and information that might prove to be useful when using the expansion board.

## 4. SYZYGY DNA

The SYZYGY DNA enables SYZYGY peripherals to convey crucial information to the carrier. This includes voltage ranges as well as essential identifying information such as the manufacturer's name, part number and serial number.

## 4.2 peripheral MCU (pMCU)

The Physical Device attached to the I2C signals on the peripheral, known as the Peripheral MCU (pMCU), plays a central role. It measures the voltage on the Rga pin shortly after startup and determines its I2C address based on a predefined table outlined in the manual.

## 4.3 Usage of I2C protocol

The communication between the SYZYGY peripheral and the carrier is done through an I2C-compatible protocol. This allows for efficient data exchange, enabling the peripherals to convey crucial information.

## Data transfer process

Read operations in the SYZYGY DNA framework initiate with a write transaction to set the sub-address for subsequent reads. This information is provided for guidance, assisting peripheral manufacturers in configuring their peripherals effectively.

Upon acknowledgment of the write operation, the SmartVIO controller writes the high and low bytes of the desired sub-address. The MCU acknowledges each received byte, ensuring valid data transmission. The operation concludes with an I2C stop condition.

# 5 Appendix

Throughout the research process, the manufacturer's official documents served as the primary source of information, except for specific details that fell beyond the scope covered by these documents.

Pcb-template([link](https://github.com/SYZYGYfpga/pcb-templates?tab=readme-ov-file))

ZUBoard 1CG([link](https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/zuboard-1cg/))

Syzygy DNA specifications([link](https://syzygyfpga.io/wp-content/uploads/2020/05/Syzygy-DNA-Specification-V1p1.pdf))

Syzygy carriers([link](https://syzygyfpga.io/carriers/))

Syzygy specifications([link](https://syzygyfpga.io/wp-content/uploads/2020/05/Syzygy-Specification-V1p1.pdf))

Syzygy interface([link](https://syzygyfpga.io/wp-content/uploads/2020/05/Syzygy-Specification-V1p1.pdf))